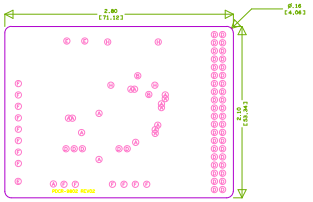
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	INITIAL RELEASE	09/23/10	RKAD
2	DIODE CONNECTIONS,SILK CHANGES	11/26/10	RKAD





DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
⊗	12.0	+3.0/-3.0	PLATED	16
⊛	20.0	+0.0/-0.0	PLATED	2
⊚	40.0	+0.0/-0.0	PLATED	45
⊜	43.0	+0.0/-0.0	PLATED	3
⊝	56.0	+3.0/-3.0	PLATED	14
⊞	70.0	+3.0/-3.0	PLATED	4

NOTES:(UNLESS OTHERWISE SPECIFIED)

1. RoHS COMPLIANT CERTIFICATION OR MATERIAL DECLARATION REQUIRED
2. MATERIAL:
   A. IS410 OR EQUIVALENT. MATERIAL MUST CONFORM TO UL94V-0.
   B. USE HTE COPPER. AS SPECIFIED IN THE CROSS SECTION DIAGRAM
   C. OVERALL METAL TO METAL THICKNESS AS SPECIFIED IN THE CROSS SECTION
3. DRILLING:
   A. DIAMETERS IN DRILL TABLE ARE FINISHED HOLE SIZES +/-.003 tol.
      UNLESS OTHERWISE SPECIFIED IN DRILL TABLE.
   B. TEARDROP ALLOWED ON ENTRY OF VIA ON EVERY TRACE LAYER.
4. PLATING:
      COPPER PLATING IN THRU-HOLES .001 min.
5. MARKING:
   A. SILKSCREEN IN WHITE NON-CONDUCTIVE EPOXY INK ON PRIMARY SIDE OF THE
      BOARD OR BOTH SIDES IF APPLICABLE.
   B. FABRICATOR TO PLACE DATE CODE AND LOGO ON SECONDARY SIDE IN ETCH
      (PREFERRED) OR SILKSCREEN.
6. FINAL FABRICATION:
   A. SOLDRMASK PRIMARY AND SECONDARY SIDE OF BOARD USING LIQUID PHOTOIMAGABLE
      MASK MATERIAL OVER BARE COPPER. PER IPC-SM-840. MASK ARTWORKS PROVIDED
      ARE 1:1. SOLDERMASK COLOR **BLUE**
7. FINISH:
   A. SHALL BE ELECTROLYTIC NICKEL/GOLD. ELECTROLESS NIKEL / IMMERSION GOLD. (ENIG)
   B. NICKEL THICKNESS: 100-200 MICROINCHES.
   C. GOLD THICKNESS: 3-10 MICROINCHES.
8. BOARDS SHALL BE PURCHASED FROM UL RECOGNIZED VENDORS ONLY AND SHALL BE
   MARKED IN COPPER ON SECONDARY SIDE OF BOARD WITH VENDORS UL IDENT.
   FLAMABILITY RATING (94-V0), DATE CODE (WWYY), AND RoHS COMPILANT SYMBOL.
9. MANUFACTURE BOARD TO BE IN ACCORDANCE WITH PERFORMANCE STANDARD
   IPC-6011/6012 CLASS 2 BOARD TO BE INSPECTED PER IPC-600-A CLASS 2.
10. MAXIMUM WRAP OR TWIST SHALL NOT EXCEED .010 in/in.
11. TESTING:
   A. FABRICATOR TO ADD TEST STRUCTURES OR CUPONS AS NEEDED.
   B. T-LINE IMPEDENCE TO BE TESTED OR GURANTEED WITHIN 10% IF SPECIFIED IN
      THE CROSS SECTION. TOLERANCE TO BE +/-10% UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE
DIMENSIONS ARE IN INCHES	DRAWN :	
TOLERANCES ON: ANGLES +/- 2°	CHECKED : RKAD	11/26/10
2 PL DECIMALS +/- .010	ENGRG : PFZ	11/26/10
3 PL DECIMALS +/- .005	ISSUED	
THIRD ANGLE PROJECTIONS		

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FABRICATION DRAWING

CY8CKIT-025 PSoC precision Analog Temperature Sensor Expansion Kit

SIZE	FSCM NO	DWG NO	REV
C		PDC-09802	02

SCALE: 1/1 SHEET: 1 OF 1